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Specifications for the CDF II Master Clock System

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Abstract

This note summarizes specifications for the CDF II Master Clock System as a user point of view.

1 Introduction and Overview

The purpose of the CDF Master Clock system is to provide timing signals to the front-end electronics and trigger. These timing signals are to be coherent with the bunches within the Tevatron and have good stability and jitter characteristics. After a brief overview of the CDF Master Clock system, this note describes timing of the Clock signals and the current accelerator running plan(section 2), distribution scheme (section 3), and stability and jitter characteristics (section 4).

The Run II CDF Master Clock system is very similar to the Run I D0 Clock system [1]. For Run II, the hardware of the CDF and D0 Clock systems are essentially identical except for specific fanout modules. The hardware of the Run II Clock system is being designed and built by Steve Chappa (Fermilab). Several documents on the Run II CDF Master Clock System and related issues have been written by Steve (see reference [2],[3],[4],[5], [6],[7]) and for technical details please refer to these documents.

In Run II CDF, with the exception of the silicon systems (SVX II and ISL), all subsystems which require the Clock signals (including the trigger system) receive the CDF Clock signals via the "TRigger And Clock + Event Readout" (TRACER) modules [8]. The TRACER module receives 4 different timing signals (CDF_CLK, B_Cross, B_Zero, and Abort_Gap signals) from the Master Clock system. Each TRACER module, then, distributes these signals by driving them onto the CDF custom backplane (see CDF/DOC/TRIGGER/CDFR/2388) in a standard 21-slot commercial VME crate. Hence the Clock signals are available to all modules plugged into the VME crate. The TRACER does not do any timing adjustment to the signals from the Master Clock, except for one alteration which is to symmetrize the

CDF_CLK (132 ns) signal. The CDF_CLK signal which is received by the subsystem users from the backplane is then symmetric, though the CDF_CLK signal input to the TRACER module from the Master Clock system is not.

Silicon detector systems are read out by the SRC (Silicon Readout Controller) module [9]. The SRC receives the Clock signals directly from the Master Clock System. In addition to the 4 signals* (CDF_CLK, B_Cross, B_Zero, and Abort_Gap signals) which the TRACER receives, the CDF Master Clock system sends a 53 MHz Clock signal (53_MHz_CLK) to the SRC module which is derived from the Tevatron RF system.

The Master Clock system is set up to deliver the Clock signals to every system with the same timing (within ± 1 nsec). This means that the SRC and the TRACER modules receive all the Clock signals in phase regardless of their locations. However, in a CDF crate which contains a TRACER module, there is a slot to slot propagation delay (order of 7 nsec at 20 slots away from the TRACER) at the backplane of the crate, and this propagation delay is not corrected by the TRACER.

2 Timing of Signals

2.1 CDF Master Clock Signals

The 53_MHz_CLK signal is derived from the Tevatron RF system and is NOT a programmed signal. The 53_MHz_CLK signal is only sent to the SRC module. The other four signals are programmed† by the Sequencer Module [1] [2]. These four programmed signals are distributed to both the SRC and the TRACER modules. The timing diagram of these signals is shown in Figure 1. A description of the signals is given below. The Master Clock System uses an "active high" convention. The Master Clock output signals shown in the top half of Figure 1 follow this "active high" convention. However, the TRACER which uses TTL logic, outputs "active low" signals to the backplane. The TRACER output of the Clock signals are illustrated in the bottom half of Figure 1.

53_MHz_CLK: 53.103 MHz, 18.83 nsec (= one RF bucket) signal
with a 50 % duty cycle (often written as 53MHz, 19 nsec).
This signal is the root Clock signal that all programmed
signals are derived from. All the programmed signals are
timed at a rising edge of this 53_MHz_CLK signal.
One revolution corresponds to 1113 RF buckets.

*Currently, the exact same timing of the 4 signals are planned for both SRC and TRACER. The Master Clock Sequencer, however, could provide differently timed signals to each system.

†Sequencer module drives up to 23 output signals whose state at each of the 1113 RF buckets is determined by a programmed lookup memory. We plan to use 4 out of 23 possible programmed outputs.

CDF_CLK: This signal is a 132 ns Clock signal and sometimes called "Master_Clock".
This signal is programmed with a period of seven RF buckets. Currently a 1/7 (1 bucket up, 6 buckets down) duty cycle is planned from the output of the Master Clock system, sending it to the SRC and TRACER modules. The TRACER module will symmetrize this CDF_CLK signal to 50% duty cycle. Hence, all the modules which receive the signals from the TRACER will see the symmetric CDF_CLK signal.

B_Cross: This signal is programmed and contains a two-bucket width pulse for each bunch that is predicted to be in the Tevatron. When the accelerator is running in the 132 ns mode this signal is expected every 132 ns except during the Abort_Gap periods when there are no bunch crossings. When the accelerator is running in the 395 ns mode, this signal is expected every 395 ns except during the Abort_Gap periods. We plan to program the B_Cross signal such that the leading edge of this signal will precede the leading edge of CDF_CLK by 19 ns (one bucket) and stay high for another 19 ns (one bucket) after the leading edge of the CDF_CLK signal. The timing of this signal will be common to all the subsystems.
This signal is used to gate front-end ADCs and TDCs, and by the TS to gate the Level 1 accept.

B_Zero: This signal is programmed and contains a two-bucket width pulse. The placement of this pulse is programmed to correspond to a bunch that is designated to be the "first" bunch in the revolution. The B_Zero signal comes once every 159 CDF_CLK cycle (= 1113 buckets).
We plan to program the B_Zero signal such that the leading edge of this signal will precede the leading edge of CDF_CLK by 19 ns (one bucket) and stay high for another 19 ns (one bucket) after the leading edge of the CDF_CLK signal. The timing of this signal will be common to all the subsystems.
This signal is used to synchronize the front-end pipelines following a reset operation.

Abort_Gap: This is also a programmed signal. This signal indicates the presence of an abort gap. The Abort_Gap signal is high during an abort gap and Abort_Gap is low when B_Cross is present. A typical Abort_Gap is 139 RF buckets in length ($\approx 2.6\ \mu$ sec).
Exact timing of when to turn on/off the Abort_Gap with respect to the leading edge of the CDF_CLK signal will be determined depending on the needs of the subsystems.
As a proposal, we are currently planning to program the Abort_Gap signal such that the Abort_Gap turns high 38 ns (two buckets) prior to the leading edge of the CDF_CLK signal which corresponds the first empty bucket which would be filled if there were not an abort gap. The Abort_Gap signal will turn off 19 ns (one bucket) prior to the leading edge of the first B_Cross signal after the abort gap, and thus 38 ns (two buckets) prior to the leading edge of the corresponding CDF_CLK signal (see Figures 1 and 2).
The Abort_Gap signal is used by the SVX system to reset the front-end amplifiers to baseline. This information is also used by TSI to generate calibration triggers for the calorimeter light pulser system during a data-taking run.

2.2 Current Plan of Accelerator Running Mode

The information in this subsection has been provided mainly by Paul Derwent.

Currently, at the beginning of Run II, a three fold symmetry is assumed in the accelerator operation. There would be three abort gaps with 139 RF buckets in length each ($\approx 2.6\mu$sec) and three active time periods between the abort gaps, each with 232 RF buckets in length. (There are 1113 RF buckets total in one revolution. The frequency of RF is 53.103 MHz, 18.83 nsec per bucket.) Within an active time period, there are 12 beam crossings which occur once every 21 RF buckets (395 nsec operation mode). Hence, there are 36 beam crossings in a revolution ("active time period with 12 Crossings + abort gap" repeated 3 times). The CDF Master Clock system receives the TEV Marker signal once a revolution. Using this information, the B_Zero signal will be programmed to correspond to the first beam crossing which comes once per revolution. Figure 2 shows the 1/3 of the Tevatron revolution with beam crossings indicated by filled circles. Figure 2 also shows timing of the 53_MHz_CLK and the four programmed Clock signals at the boundaries of an active time period and an abort gap.

The web page:

http://www-fermi3.fnal.gov/run2/chapter6/Chapter6.html

describes the Tevatron performance and projections. In particular, subsection 6.5.2 has a discussion of where the proton and anti-proton bunches are in time. This web page is undergoing revision, however, according to the current plan, the timing of the Clock signals will stay the same.

3 Distribution Scheme

Since the Master Clock system is designed for both CDF and D0 experiments, there are some features that the Clock system has but we do not use. More complete functionality of each of the modules in the Master Clock System can be found in references [1] and [2]. Here, we focus on CDF II Master Clock system configuration and operation.

3.1 Configuration

Figure 3 shows the CDF II Clock signal distribution scheme.

On the 2nd floor of the B0 assembly building, we plan to have a single 7 ft. relay rack (The Master Clock Rack) which contains all the necessary modules for the Master Clock system except the CDF Clock Fanout modules. The CDF Clock Fanout modules, housed in CDF Clock Fanout Crates, are located in the 1st floor, 2nd floor, and the collision hall. In the Master Clock Rack there is a NIM crate which deals with the Tevatron interface section. There is also a VME Master Clock Crate. This crate contains the main part of the Master Clock system which consists of three module types: the Phase Coherent Clock (PCC) module, the Sequencer module, and Selector Fanout Module (SFM). The backplane of this crate is designed specially to facilitate the Clock operation.

The PCC module phase locks a 53 MHz oscillator to an RF signal from the Tevatron. This, together with a marker signal, is input to the Sequencer module. A Sequencer module drives up to 23 output signals whose state at each of the 1113 RF buckets is determined by a programmed lookup memory. The PCC module is capable of driving up to 3 separate Sequencer modules. For the CDF Clock operation, we plan to use one PCC and one Sequencer module. Hence, the maximum number of programmed signals is limited to 23. Our current plan is to use either 4 or 12 (3 sets of 4 for the 3 different locations) programmed signals in total depending on how we adjust the delays (see section 3.2). If, for some reason, we need more than 23 programmed signals, we would need another Master Clock Rack in the 2nd floor and a more complex distribution scheme must be designed and built.

The SFM selects four signals of the 23 programmed signals from the Master Clock Crate's backplane and drives the outputs to the CDF Clock Fanout crates. In addition to the selected four programmed outputs, the SFM can also output the 53_MHz_CLK signal. Another feature of the SFM is "retiming". The set of four

signals selected by the SFM module can be adjusted over the range of 16 nsec with a resolution of 1 nsec. This timing adjustment is done commonly to all four selected signals, not independently to each signal. We only plan to use this feature to make a fine timing adjustment such that the leading edges of the programmed signals will be in phase with the 53_MHz_CLK signal. We are not planning to have any programmed signals which would be out of phase with the 53_MHz_CLK signal. In the Master Clock Crate, we could have a maximum of 13 SFM modules.

In addition to above, there will be a module called the Accelerator Synchronization Controller Module (ASC) in the Master Clock System. This is a 6U VME Module. The purpose of the ASC module is to monitor and compensate for the long term drift of the TEV signals. Currently, there are several proposed operation modes for this module. However, the precise design has not yet been done.

From the SFM modules, the sets of 4 Clock signals and the 53_MHz_CLK are sent to the CDF Fanout modules. The TRACER and SRC modules receive the Clock signals from the CDF Fanout modules' outputs. The CDF Fanout Crates which distribute the output signals to the TRACERs will be located in the 1st floor counting room, 2nd floor trigger room and the collision hall. The CDF Fanout Crate which distributes the output signals to the SRC will be located only in the 1st floor counting room. The CDF Fanout modules are strictly hardware and there is no software communication to these devices. Each module has a fanout capability of two outputs and one CDF Fanout Crate holds a maximum of 19 CDF Fanout modules. There will be vernier timing adjustments on-board. Each Fanout module has the ability to adjust each fanned out signal over a rage of 16 ns with a resolution of 0.5 ns. This is mainly to compensate for cable skews and backplane delays in the CDF Fanout crates. We plan to adjust the timing at the fanout modules only once during the installation stage. The CDF Fanout modules receive ECL level inputs and output LVDS level signals which are sent to the SRC and TRACER modules.

3.2 Signal Types, Cables, Connectors, etc.

The differential ECL (DECL) signal type is used for all signals from the Master Clock System to the CDF Fanout modules (corresponds to the sets of cables A, Bs, Bt, and C in Figure 3.) A custom specified twinax cable manufactured by Consolodated Wire Co. will be used for the signals. The connector for the twinax cable will be a triaxial connector made by Trompeter.

We are considering two ways which would achieve our timing constraints[‡]: One way is to have only one set of 4 Clock signals and have all the cable lengths (cable sets A, Bs, Bt, and C) be the same. The other is to have three sets of 4 Clock signals (one set for the 2nd floor, one set for the 1st floor, and one set for the collision

[‡]The Master Clock system is set up to deliver the Clock signals to every system with the same timing (within ± 1 nsec). Hence, the SRC and the TRACER modules receive all the Clock signals in phase regardless of their locations.

hall) which are programmed to allow for the differences in the cable length such that all the signals will arrive at the CDF Fanout crates in phase. Both solutions would satisfy the goal. The latter has the advantage of not having long cables coiled up in the 1st and 2nd floor. The cable length needed for the cable set C (to the collision hall) is estimated to be $\approx$ 185 ft.

The cables indicated by D in Figure 3 carry the four programmed signals from the CDF Fanout crates to the TRACERs and SRCs. In addition, the SRC modules receive 53_MHz_CLK signal from the cable indicated by D53 in Figure 3. The signal type here is LVDS for both D and D53. We plan to use Beldon E108998 twisted 4-pair cable [6]. These cables (cable D and D53) will all be cut to the same length, $\approx$ 60 ft. They should not be longer than 75 ft[6]. The connectors used here are 8 pin AMP Shielded Data-Link type. Cable D and cable D53 will have different keys (C-key for D and E-key for D53) to prevent them from being switched at front panels. The part # of the connectors used for the cable D is 3-520459-3 and the part # for the cable D53 is 5-520459-3. The pin assignments of the connectors for the cable D and cable D53 are shown in Tables 3-1 and 3-2, respectively.

Pin	Signal
1	CDF_CLK (+)
2	CDF_CLK (-)
3	B_Cross (+)
4	B_Cross (-)
5	B_Zero (+)
6	B_Zero (-)
7	Abort_Gap(+)
8	Abort_Gap(-)

Table 3–1: Pinout of the connection to TRACER and SRC from the cable D. The signals are assumed to be "active high", so (+) corresponds to those signals shown in the top half of Figure 1.

4 Timing Resolution

The σ of the jitter value is estimated to be better than 200 ps. Here, jitter is defined as a high frequency instability of a single line. The Clock signals are assumed to arrive at all the TRACER and SRC modules at the same timing within $\pm$ 1 ns. The medium and long term stability should be maintained by the ASC module and also should be stable within $\pm$ 1 ns.

Pin	Signal
1	53_MHz_CLK (+)
2	53_MHz_CLK (-)
3	-
4	-
5	-
6	-
7	-
8	-

Table 3–2: Pinout of the connection to SRC from the cable D53. 53_MHz_CLK (+) corresponds to the 53_MHz_CLK signal shown in Figure 1.

5 Acknowledgement

I appreciate help from many people putting together this note. Especially I would like to thank Steve Chappa, Terri Shaw, Aesook Byon, Peter Willson, Paul Dewent, Colin Gay and Steve Vejcik.

References

[1] C. Rotolo *et al.*, Proc. IEEE Nucl. Sci. Symp. (1991).

[2] "CDF Clock System Upgrades, Upgrade Proposal",S. Chappa, April, 1994, revised June 1996.

[3] "Drift Study of the TVBS and TVBS_F signals", S. Chappa, D0 Note #2721, Sep. 8, 1995

[4] "CDF Clock System Upgrades, Comparison of LVDS and DECL Differential Drive Capability" S. Chappa, May 17, 1996.

[5] "CDF Clock System Upgrades, LVDS Drive Capability Beldon E89504 Cable Test", S. Chappa, June 7, 1996.

[6] "CDF Clock System Upgrades, LVDS Drive Capability Beldon E108998 Cable Test", S. Chappa, June 13, 1996.

[7] "CDF Clock System Upgrades, Cost and Manpower Estimates", S. Chappa, July 11, 1996.

[8] "Specification for TRigger And Clock + Event Readout (TRACER) modules", T. Shaw, Apr. 19, 1993, revised Aug. 19, 1997. ftp://www-ppd.fnal.gov/ett_ftp/CDF_DOCS/TRACER/.

[9] "Silicon Readout Controller, Technical Design Report", Harvard Group, Dec. 9, 1996. ESE project index # HAR-SVX-960210, http://heplsgi1.harvard.edu/maria/src/dec8.ps

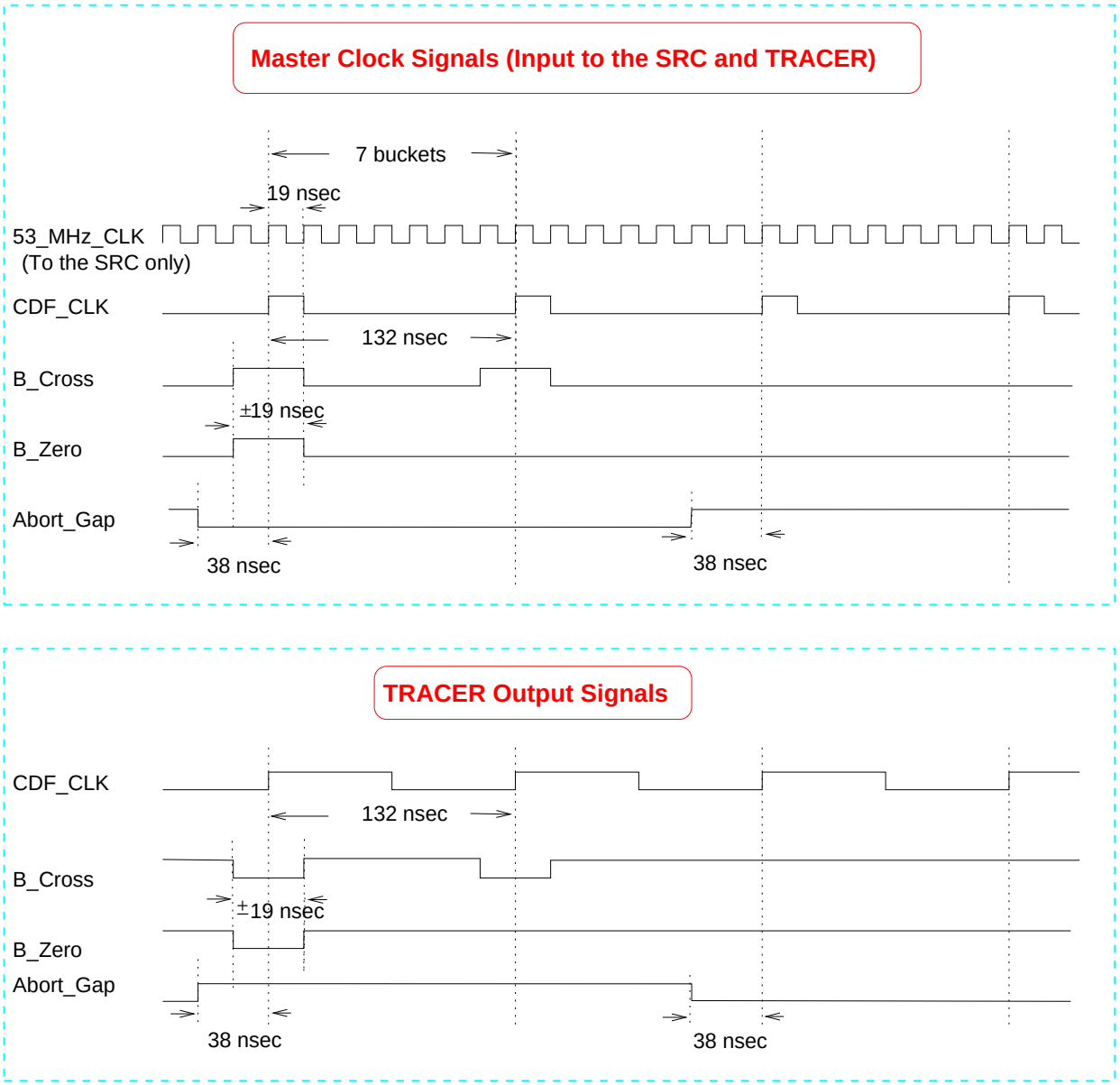

Figure 1: Timing of 53_MHz_CLK signal and the 4 programmed Clock signals at the SRC and TRACER input, and the TRACER output. This figure is shown for the 132 ns operation mode. In the case of the 395 ns operation, B_Cross signal comes every 3rd CDF_CLK cycle. Please note that the Abort_Gap signal will most likely not come as soon after the B_Zero signal as indicated in this diagram (See section 2.2 for the current accelerator plan and also Figure 2). This is done for illustrative purposes.

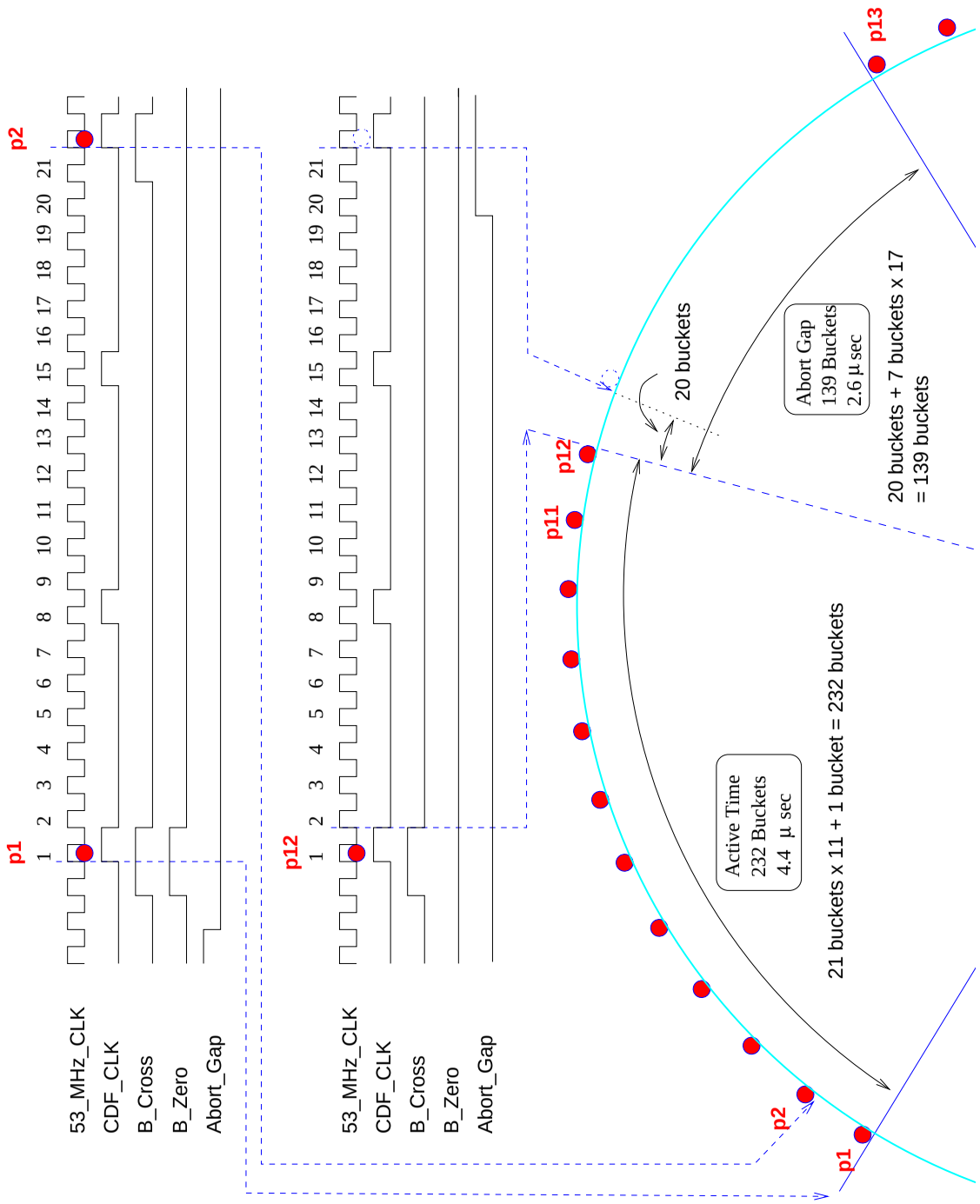

Figure 2: This figure shows 1/3 of the Tevatron revolution with the beam crossings indicated by filled circles for the 395 nsec operation. The open dashed circle indicates the first empty bucket which would be filled if there were not an abort gap. This figure also shows timing of the 53_MHz_CLK and the four programmed Clock signals at the boundaries of an active time period and an abort gap.

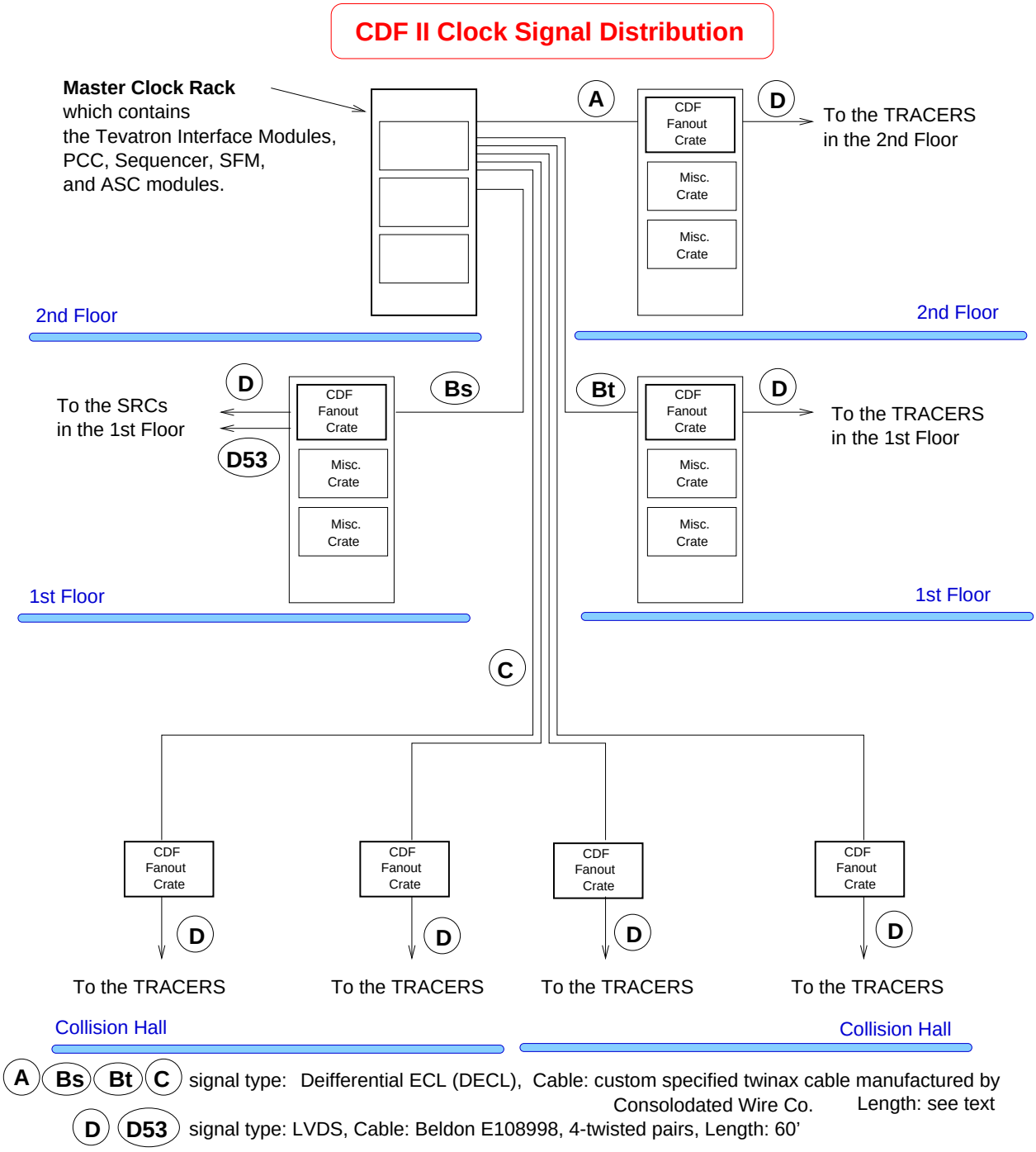

Figure 3: CDF II Master Clock signal distribution scheme.